deposition. Additionally, the layer **365** may be planarized, for example, by means of a known chemical mechanical polishing process.

[0084] The present disclosure is not restricted to embodiments wherein ion-implanted regions are formed in each of the material layers **370**, **382** and in the liner layers **380**, **381**. Moreover, ion-implanted regions need not be formed in the material layer **382** both before the formation of the sidewall spacer structures **383**, **483** and after the formation of the sidewall spacer structures **383**, **483**. In other embodiments, one or more of the ion implantation processes performed to create ion-implanted portions of the material layers **370**, **382** described above may be omitted. Moreover, the present disclosure is not restricted to embodiments wherein two sidewall spacer structures are formed adjacent each of the gate electrodes **306**, **406**. In other embodiments, only one sidewall spacer structure may be formed adjacent each of the gate electrodes **306**, **406**, similar to the method according to the state of the art described above with reference to FIGS. **1***a*-**1***d*. In still further embodiments, three or more sidewall spacer structures may be formed adjacent each of the gate electrodes **306**, **406**.

[0085] The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

What is claimed:

1. A method of forming a semiconductor structure, comprising:
- providing a semiconductor substrate, a feature being formed over said substrate, said feature having a side surface and a top surface;
- forming a material layer over said substrate, said material layer covering at least said side surface of said feature;
- performing an ion implantation process to create an ion-implanted portion in said material layer; and
- performing a first etch process adapted to remove said ion-implanted portion in said material layer at a greater etch rate than other portions of said material layer.

2. The method of claim **1**, wherein said formation of said material layer comprises:
- depositing said material layer over said substrate; and
- performing an anisotropic second etch process to remove portions of said material layer over said top surface of said feature.

3. The method of claim **2**, wherein said feature comprises a gate electrode, and wherein said second etch process is adapted such that a portion of said material layer remains over said side surface to form a sidewall spacer structure adjacent said gate electrode.

4. The method of claim **1**, wherein said material layer is provided over said top surface and said side surface, and wherein said ion-implanted portion is formed over said top surface.

5. The method of claim **4**, wherein a portion of said material layer over said top surface is removed by said etch process.

6. The method of claim **5**, wherein said feature comprises a gate electrode, and wherein said first etch process is adapted such that a portion of said material layer remains over said side surface to form a sidewall spacer structure.

7. The method of claim **1**, wherein said first etch process comprises a wet etch process.

8. The method of claim **1**, wherein said first etch process comprises a dry etch process.

9. The method of claim **8**, wherein said first etch process is anisotropic.

10. A method of forming a semiconductor structure, comprising:
- providing a semiconductor substrate, a gate electrode being formed over said substrate, said gate electrode having a top surface and a side surface;
- depositing a first material layer over said top surface and said side surface;
- performing a first ion implantation process to create a first ion-implanted portion in said material layer over said top surface of said gate electrode; and
- performing a first etch process adapted to remove said first ion-implanted portion at a greater etch rate than other portions of said first material layer, said etch process being stopped upon a removal of a portion of said first material layer over said top surface such that portions of said first material layer over said side surface form a first sidewall spacer structure adjacent said gate electrode.

11. The method of claim **10**, further comprising forming a second sidewall spacer structure adjacent said first sidewall spacer structure.

12. The method of claim **11**, wherein said formation of said second sidewall spacer structure comprises:
- depositing a second material layer over said top surface and said side surface;
- performing a second ion implantation process to create a second ion-implanted portion in said second material layer over said top surface; and
- performing a second etch process adapted to remove said second ion-implanted portion at a greater etch rate than other portions of said second material layer, said second etch process being stopped prior to complete removal of said second material layer.

13. The method of claim **11**, further comprising:
- performing a second ion implantation process to create a second ion-implanted portion in said second sidewall spacer structure; and
- performing a second etch process adapted to remove said second ion-implanted portion at a greater etch rate than other portions of said second sidewall spacer structure.

14. The method of claim **10**, wherein a direction of incidence of ions in said ion implantation process is substantially perpendicular to said top surface.

15. The method of claim **10**, further comprising depositing a layer of a dielectric material over said substrate.

16. The method of claim **14**, wherein said layer of dielectric material comprises an intrinsic stress.

17. A method of forming a semiconductor structure, comprising:
- providing a semiconductor substrate comprising a gate electrode and a sidewall spacer structure formed adjacent said gate electrode;